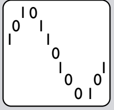
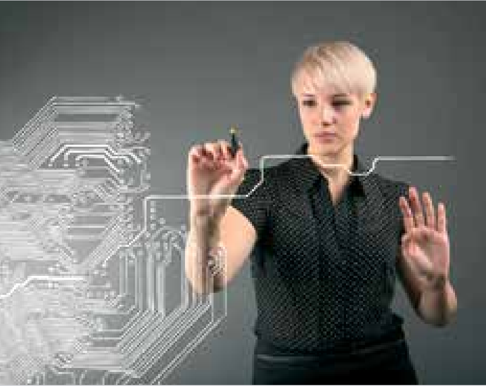


Enabling technologies for heterogeneous systems

MEDEA+

2T405 Chip/package-system co-design (CoSiP)



Making SiP design data more easily recyclable

Design runs for electronic chips, packages and printed-circuit boards have historically been separate processes. Yet market demand is pushing the development of ever more compact electronic systems, where integrating the various analogue and digital component parts becomes a single design process. 'Co-design' or integrating the three different design streams for chips, packages and boards into a single process has therefore become a key goal for European semiconductor companies. And developing an efficient and functioning co-design approach was the target of the MEDEA+ CoSiP project.

Co-design methodology, or concentrating the design of semiconductor chips, packages and systems into a single integrated process, has long been a key target for the European semiconductor industry. Achieving this target has grown in importance as new system-in-package (SiP) and system-on-chip (SoC) designs integrate more and more analogue components in order to build compact modern electronic systems.

To date, however, design runs for new chips, packages and printed-circuit boards (PCBs) have been treated as separate and independent processes. Chip development has been coupled with neither package nor PCB design, while package development was isolated both from chip design and PCB development.

The MEDEA+ 2T405 CoSiP project therefore aimed to create an integrated design platform that would embrace all three integration levels: chip, package and board. CoSiP focused on the development of an SiP design platform especially for heterogeneous system integration in order to enable fast, efficient and cost-effective development of complex, heterogeneous compact systems.

No standard EDA landscape

CoSiP came at the right time. Co-design methodology, data management and tooling are becoming increasingly important to the semiconductor design and manufacturing industry, as more and more analogue components need to be integrated with their digital bedfellows in modern electronic systems.

To date however, there has been little focus on chip/package co-design applying SiP technologies in Europe. Co-design is an important prerequisite for all types of SiP projects – as well as for SoC, where advanced packaging solutions are required. It is a fundamental requirement if 3D technologies are to be used to model new product development.

The situation has been further complicated by the lack of a standard electronic design automation (EDA) landscape. The major EDA vendors around the world – mostly US – support only proprietary interfaces and data models. This means that major global users all have their own design flows, with little interoperability between them. CoSiP was intended as a solution to this problem, in the process achieving more independence for the European semiconductor sector from proprietary design offerings.

Data backbone concept

CoSiP came up with a number of key approaches that allowed designers to simulate complete semiconductor systems. The MEDEA+ project succeeded particularly in modelling the interaction between different domains such as

application-specific integrated circuits, sensors, packages, boards and mechanical components.

During the project, the partners in close contact with the major EDA vendors decided not to go for a standardised chip/package/board design database as originally planned, because of the overhead involved in maintaining a common standard every time one partner's design process changed. Instead, CoSiP came up with an alternative solution – a 'data backbone' which would support more efficient file-based collaboration.

The CoSiP data backbone then became the central concept around which the new design approaches and tools were built. Essentially, it links the data in all the different design processes via an XML language interface, making the data developed in one design project easily transferable to a completely different one.

This new concept has greatly simplified data exchange between the different chip, package and board design processes, underpinning the spread of a new first-time right approach to SiP design. Previously, each time development started on a new project the design process would have to start from scratch, and any data from other design processes re-entered manually, with all the risks of human error that this implies. The data-backbone XML interface has enabled direct electronic import of much of this data from other processes, bringing significant savings in time and development effort.

Data more easily recyclable

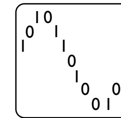
The switch from the idea of developing a unified database to a shared data backbone has enabled the CoSiP partners to incorporate the results of the project quickly and easily into their production processes. At the same time, the project has been able to overcome many of the issues involved in simulating heterogeneous SiP architectures.

The results of CoSiP have also been a door opener for European small and medium-sized enterprises and research institutes. The data-backbone approach enables them to overcome many of the blocking restrictions on flexibility caused by existing proprietary EDA standards, and to develop new design approaches and tools that connect more easily to industrial design flows.

Society will require compact semiconductor-system solutions in many fields if the promise of future electronic technologies is to be delivered. Communications, transport, healthcare, pharmacy, biochemistry, education, agriculture, environmental control, weather forecasting and recycling all stand to benefit in some way.

CoSiP has developed an approach to answering these needs in a much faster way. The data-backbone concept makes the data developed in one design project more easily recyclable in another, in the process delivering a significant boost to the abilities of the European semiconductor industry.

Chip/package/system co-design is a must if European semiconductor companies are to tackle the increasing complexity of compact systems and the new nanotechnologies. Integrated circuit design remains an important European strength; this MEDEA+ project has boosted SiP design capabilities in a way that will help European companies retain their market position for some time to come.



2T405 Chip/package-system co-design (CoSiP)

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PROJECT LEADER:

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KEY PROJECT DATES:

Start: June 2008
End: December 2011

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.